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#sjplacer

#Version: 1.1

#Build Date: Dec 5 2017 15:35:27

#File Generated: Aug 19 2019 18:32:42

#Purpose:

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Executing : C:\Program Files (x86)\Cypress\PSoC Creator\4.2\PSoC Creator\bin/sjplacer.exe --proj-name IDAC8\_Example01 --netlist-vh2 IDAC8\_Example01\_p.vh2 --arch p35\_udb4x6 --arch-file C:\Users\sebas\Documents\PSoC Creator\4.2\Devices\arch/udbdsi\_4x6\_24.cydata --ip-file C:\Users\sebas\Documents\PSoC Creator\4.2\Devices\psoc5/psoc5lp/ip\_blocks.cydata --rrg-file C:\Users\sebas\Documents\PSoC Creator\4.2\Devices\psoc5/psoc5lp/route\_arch-rrg.cydata --irq-file C:\Users\sebas\Documents\PSoC Creator\4.2\Devices\psoc5/psoc5lp/irqconn.cydata --drq-file C:\Users\sebas\Documents\PSoC Creator\4.2\Devices\psoc5/psoc5lp/dmaconn.cydata --dsi-conn-file C:\Users\sebas\Documents\PSoC Creator\4.2\Devices\psoc5/psoc5lp/dsiconn.cydata --pins-file pins\_68-QFN.xml --lib-file IDAC8\_Example01\_p.lib --sdc-file IDAC8\_Example01.sdc --io-pcf IDAC8\_Example01.pci --outdir .

Softjin Techologies Placer, Version 1.1

Build Date : Dec 5 2017 15:33:41

D2004: Option and Settings Summary

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Netlist vh2 file - IDAC8\_Example01\_p.vh2

Architecture file - C:\Users\sebas\Documents\PSoC Creator\4.2\Devices\arch/udbdsi\_4x6\_24.cydata

Package -

Defparam file -

SDC file - IDAC8\_Example01.sdc

Output directory - .

Timing library - IDAC8\_Example01\_p.lib

IO Placement file - IDAC8\_Example01.pci

D2050: Starting reading inputs for placer

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D2065: Reading netlist file : "IDAC8\_Example01\_p.vh2"

D2065: Reading arch file : "C:\Users\sebas\Documents\PSoC Creator\4.2\Devices\arch/udbdsi\_4x6\_24.cydata"

D2051: Reading of inputs for placer completed successfully

D2053: Starting placement of the design

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Phase 2

Phase 3

Design Statistics after Packing

Number of Combinational MCs : 9

Number of Sequential MCs : 16

Number of DPs : 3

Number of Controls : 1

Number of Status : 2

Number of SyncCells : 0

Number of count7cells : 1

Device Utilization Summary after Packing

Macrocells : 25/192

UDBS : 4/24

IOs : 3/72

D2088: Phase 3, elapsed time : 0.0 (sec)

Phase 4

D2088: Phase 4, elapsed time : 0.0 (sec)

Phase 5

D2088: Phase 5, elapsed time : 0.0 (sec)

Phase 6

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Placement Timing Summary

The timing summary is based on estimated routing delays after

placement. For final timing report, please carry out the timing

analysis after routing.

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Clock Summary

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Number of clocks: 11

Clock: ADC\_DelSig\_1\_Ext\_CP\_Clk | Frequency: N/A | Target: 24.0 MHz

Clock: ADC\_DelSig\_1\_Ext\_CP\_Clk(routed) | Frequency: N/A | Target: 24.0 MHz

Clock: ADC\_DelSig\_1\_theACLK | Frequency: N/A | Target: 0.6 MHz

Clock: ADC\_DelSig\_1\_theACLK(fixed-function) | Frequency: N/A | Target: 0.6 MHz

Clock: CyBUS\_CLK | Frequency: 46.5 MHz | Target: 24.0 MHz

Clock: CyILO | Frequency: N/A | Target: 0.0 MHz

Clock: CyIMO | Frequency: N/A | Target: 3.0 MHz

Clock: CyMASTER\_CLK | Frequency: N/A | Target: 24.0 MHz

Clock: CyPLL\_OUT | Frequency: N/A | Target: 24.0 MHz

Clock: UART\_1\_IntClock | Frequency: 46.5 MHz | Target: 0.5 MHz

Clock: \ADC\_DelSig\_1:DSM\/dec\_clock | Frequency: N/A | Target: 0.1 MHz

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End of Clock Summary

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D2088: Phase 6, elapsed time : 0.0 (sec)

Phase 7

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Clock Summary

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Number of clocks: 11

Clock: ADC\_DelSig\_1\_Ext\_CP\_Clk | Frequency: N/A | Target: 24.0 MHz

Clock: ADC\_DelSig\_1\_Ext\_CP\_Clk(routed) | Frequency: N/A | Target: 24.0 MHz

Clock: ADC\_DelSig\_1\_theACLK | Frequency: N/A | Target: 0.6 MHz

Clock: ADC\_DelSig\_1\_theACLK(fixed-function) | Frequency: N/A | Target: 0.6 MHz

Clock: CyBUS\_CLK | Frequency: 2.2 MHz | Target: 24.0 MHz

Clock: CyILO | Frequency: N/A | Target: 0.0 MHz

Clock: CyIMO | Frequency: N/A | Target: 3.0 MHz

Clock: CyMASTER\_CLK | Frequency: N/A | Target: 24.0 MHz

Clock: CyPLL\_OUT | Frequency: N/A | Target: 24.0 MHz

Clock: UART\_1\_IntClock | Frequency: 2.2 MHz | Target: 0.5 MHz

Clock: \ADC\_DelSig\_1:DSM\/dec\_clock | Frequency: N/A | Target: 0.1 MHz

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End of Clock Summary

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D2088: Phase 7, elapsed time : 0.1 (sec)

Final Design Statistics

Number of Combinational MCs : 9

Number of Sequential MCs : 16

Number of DPs : 3

Number of Controls : 1

Number of Status : 2

Number of SyncCells : 0

Number of count7cells : 1

Number of IOs : 3

Device Utilization Summary

Macrocells : 25/192

IOs : 3/72

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Placement Timing Summary

The timing summary is based on estimated routing delays after

placement. For final timing report, please carry out the timing

analysis after routing.

======================================================================

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Clock Summary

======================================================================

Number of clocks: 11

Clock: ADC\_DelSig\_1\_Ext\_CP\_Clk | Frequency: N/A | Target: 24.0 MHz

Clock: ADC\_DelSig\_1\_Ext\_CP\_Clk(routed) | Frequency: N/A | Target: 24.0 MHz

Clock: ADC\_DelSig\_1\_theACLK | Frequency: N/A | Target: 0.6 MHz

Clock: ADC\_DelSig\_1\_theACLK(fixed-function) | Frequency: N/A | Target: 0.6 MHz

Clock: CyBUS\_CLK | Frequency: 2.2 MHz | Target: 24.0 MHz

Clock: CyILO | Frequency: N/A | Target: 0.0 MHz

Clock: CyIMO | Frequency: N/A | Target: 3.0 MHz

Clock: CyMASTER\_CLK | Frequency: N/A | Target: 24.0 MHz

Clock: CyPLL\_OUT | Frequency: N/A | Target: 24.0 MHz

Clock: UART\_1\_IntClock | Frequency: 2.2 MHz | Target: 0.5 MHz

Clock: \ADC\_DelSig\_1:DSM\/dec\_clock | Frequency: N/A | Target: 0.1 MHz

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End of Clock Summary

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Phase 6

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Placement Timing Summary

The timing summary is based on estimated routing delays after

placement. For final timing report, please carry out the timing

analysis after routing.

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Clock Summary

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Number of clocks: 11

Clock: ADC\_DelSig\_1\_Ext\_CP\_Clk | Frequency: N/A | Target: 24.0 MHz

Clock: ADC\_DelSig\_1\_Ext\_CP\_Clk(routed) | Frequency: N/A | Target: 24.0 MHz

Clock: ADC\_DelSig\_1\_theACLK | Frequency: N/A | Target: 0.6 MHz

Clock: ADC\_DelSig\_1\_theACLK(fixed-function) | Frequency: N/A | Target: 0.6 MHz

Clock: CyBUS\_CLK | Frequency: 2.2 MHz | Target: 24.0 MHz

Clock: CyILO | Frequency: N/A | Target: 0.0 MHz

Clock: CyIMO | Frequency: N/A | Target: 3.0 MHz

Clock: CyMASTER\_CLK | Frequency: N/A | Target: 24.0 MHz

Clock: CyPLL\_OUT | Frequency: N/A | Target: 24.0 MHz

Clock: UART\_1\_IntClock | Frequency: 2.2 MHz | Target: 0.5 MHz

Clock: \ADC\_DelSig\_1:DSM\/dec\_clock | Frequency: N/A | Target: 0.1 MHz

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End of Clock Summary

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D2088: Phase 6, elapsed time : 0.0 (sec)

Phase 7

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Clock Summary

======================================================================

Number of clocks: 11

Clock: ADC\_DelSig\_1\_Ext\_CP\_Clk | Frequency: N/A | Target: 24.0 MHz

Clock: ADC\_DelSig\_1\_Ext\_CP\_Clk(routed) | Frequency: N/A | Target: 24.0 MHz

Clock: ADC\_DelSig\_1\_theACLK | Frequency: N/A | Target: 0.6 MHz

Clock: ADC\_DelSig\_1\_theACLK(fixed-function) | Frequency: N/A | Target: 0.6 MHz

Clock: CyBUS\_CLK | Frequency: 2.2 MHz | Target: 24.0 MHz

Clock: CyILO | Frequency: N/A | Target: 0.0 MHz

Clock: CyIMO | Frequency: N/A | Target: 3.0 MHz

Clock: CyMASTER\_CLK | Frequency: N/A | Target: 24.0 MHz

Clock: CyPLL\_OUT | Frequency: N/A | Target: 24.0 MHz

Clock: UART\_1\_IntClock | Frequency: 2.2 MHz | Target: 0.5 MHz

Clock: \ADC\_DelSig\_1:DSM\/dec\_clock | Frequency: N/A | Target: 0.1 MHz

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End of Clock Summary

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D2088: Phase 7, elapsed time : 0.1 (sec)

Final Design Statistics

Number of Combinational MCs : 9

Number of Sequential MCs : 16

Number of DPs : 3

Number of Controls : 1

Number of Status : 2

Number of SyncCells : 0

Number of count7cells : 1

Number of IOs : 3

Device Utilization Summary

Macrocells : 25/192

IOs : 3/72

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Placement Timing Summary

The timing summary is based on estimated routing delays after

placement. For final timing report, please carry out the timing

analysis after routing.

======================================================================

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Clock Summary

======================================================================

Number of clocks: 11

Clock: ADC\_DelSig\_1\_Ext\_CP\_Clk | Frequency: N/A | Target: 24.0 MHz

Clock: ADC\_DelSig\_1\_Ext\_CP\_Clk(routed) | Frequency: N/A | Target: 24.0 MHz

Clock: ADC\_DelSig\_1\_theACLK | Frequency: N/A | Target: 0.6 MHz

Clock: ADC\_DelSig\_1\_theACLK(fixed-function) | Frequency: N/A | Target: 0.6 MHz

Clock: CyBUS\_CLK | Frequency: 2.3 MHz | Target: 24.0 MHz

Clock: CyILO | Frequency: N/A | Target: 0.0 MHz

Clock: CyIMO | Frequency: N/A | Target: 3.0 MHz

Clock: CyMASTER\_CLK | Frequency: N/A | Target: 24.0 MHz

Clock: CyPLL\_OUT | Frequency: N/A | Target: 24.0 MHz

Clock: UART\_1\_IntClock | Frequency: 2.3 MHz | Target: 0.5 MHz

Clock: \ADC\_DelSig\_1:DSM\/dec\_clock | Frequency: N/A | Target: 0.1 MHz

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End of Clock Summary

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Phase 8

D2088: Phase 8, elapsed time : 0.0 (sec)

D2054: Placement of the design completed successfully

I2076: Total run-time: 0.7 sec.